REMARKS

In response to the second (non-final) Office Action dated November 18, 2005, the Applicants hereby request reconsideration of the pending claims in light of the following.

STATUS OF CLAIMS

Claims 1-13 were pending.

Claims 1-3, 5-8, and 11-13 are amended.

Claims 9-10 are cancelled.

Claim 14 is newly added.

Accordingly, claims 1-8 and 11-14 are before the Examiner for consideration.

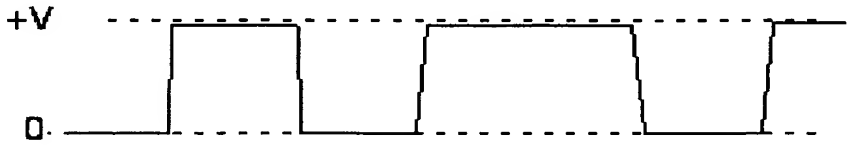
CLAIM REJECTIONS

Claims 1-13 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Pat. No. 4,408,245 to Pryor ("Pryor"). Claims 9 and 10 have been cancelled, without prejudice or disclaimer of the subject matter therein, as being generally duplicative of other claims. Claims 1-3, 5-8, and 11-13 have been amended to traverse the rejection under 35 U.S.C. § 102(b). More particularly, the Applicants respectfully submit that Pryor neither shows nor suggests each and every element/limitation of these claims, rendering them allowable over Pryor.

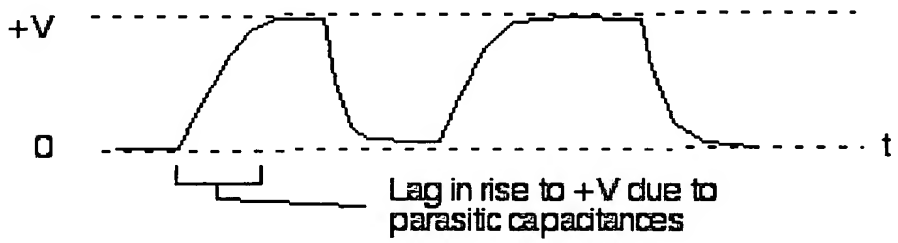
To elaborate, the present invention is generally for use in the context of a communication system that utilizes a 1-wire bus for digital communications between a transceiver-equipped processor and various devices connected to the 1-wire bus. When, for example, the processor desires to determine the status of one of the devices, it queries the device and the device sends information back to the processor/transceiver. The information is sent in digital form as a voltage signal applied to the 1-wire bus. For example, a logic "1" may correspond to a designated high voltage on the 1-wire bus, e.g., +5 V, while a logic "0" may correspond to a designated low voltage on the 1-wire bus, e.g., 0 volts. Typically, threshold voltages will be designated, such that a

voltage level above, e.g., a +4.3V threshold is considered logic "1," and a voltage level below, e.g., a +0.7V threshold is considered logic "0."

Information is transmitted serially over the bus, forming many successive high and low voltages on the bus that correspond to successive logic 1's and 0's. Ideally, the communication voltage signal would look akin to the following:



However, the devices connected to the 1-wire bus contribute a significant degree of parasitic capacitance. Because of this capacitance, the transition time from low to high voltages is significantly increased, which may lead to communication lags and errors (e.g., in effect, the capacitance has to be charged for changing the voltage level on the bus). For example, the waveform might appear roughly like the following:



To alleviate this problem, an active pull-up device may be disposed on the 1-wire bus between the transceiver and the communication devices connected to the bus. The active pull-up device is connected between ground (0 volts) and the positive power supply +Vcc. The active pull-up device detects the voltage level on the 1-wire bus. When the voltage level goes above a threshold value, as determined by measuring the voltage potential between the bus and ground, the active pull-up device switches from an internal high-impedance load (e.g., in effect connected between the bus and +Vcc) to an internal low-impedance load. This reduces the RC time constant of the impedance and parasitic capacitance in combination, causing the voltage level on the bus to much more quickly transition to the designated logic 1 level.

However, because the active pull-up device measures voltages on the bus with respect to ground (as is also the case with the transceiver and devices), errors may be introduced by system noise. As stated in the present application starting on page 4, line 28, "Even though the active pull-up device significantly reduces the adverse effects of the extra capacitance problem on the one wire bus, the communication signals are still within a noisy environment and therefore data transmitted onto the bus can still be erroneously interpreted by communication devices (I-buttons, transceivers) connected to the bus."

According to the present invention, a level shift circuit is added to the active pull-up device to mitigate this deleterious effect. The level shift circuit, e.g., a diode, is connected between ground and the input terminal of the pull-up device that is normally connected to ground. The level shift circuit is configured to produce a constant output voltage, which is applied to the active pull-up device as a constant reference voltage. (For example, a typical diode might output a +0.5V constant voltage, that is, +0.5V is the diode's constant forward bias voltage.) Thereby, instead of measuring voltage levels on the 1-wire bus with respect to ground, they are measured with respect to the constant voltage level of the level shift circuit. As stated on page 6, lines 29-31 of the present application, "As a result, the noise on the one wire data bus has a less adverse effect on the circuit's ability to detect the digital signals appearing on the one wire bus." Further, the 1-wire bus communication system is configured to operate with the constant reference voltage as a bias: "As a result [of the active pull-up device operating with reference to a voltage other than ground], the circuit operates above at least a portion of the noisy signals on the one-wire bus allowing digital signals on the bus to have a bias signal equal to the reference voltage signal. Communication devices connected to the bus are thus better able to determine the digital logic levels of the digital communication signals." Page 5, lines 18-21. As such, according to one embodiment of the present invention, not only is the active pull-up device set to operate at a constant bias voltage (by adding the level shift circuit), but the entire communication system is as well, at least in regards to communication voltage signals across the 1-wire bus.

Claims 1-3, 5-8, and 11-13 have been amended to further specify the operation and interrelationship of the active pull-up device, level shift circuit, and communication system/bus generally. For example, independent claims 1 and 7 have been amended to state: (i) that the level shift circuit provides a constant reference voltage different from the circuit ground (see, e.g., page 6, lines 25-27; page 7, lines 3-4 (it is inherent that a diode has a substantially constant forward bias voltage, i.e., constant within a small percentage due to thermal or noise variations of the current flowing into the diode)); (ii) that the active pull-up device, in effect, operates to "pull up" the voltage on the bus when it detects a low-to-high transition on the bus (see, e.g., page 4, lines 8-28)[1]; and (iii) that the active pull-up device operates with respect to the constant reference voltage in operating to pull-up the bus voltage.[2] (See, e.g., page 6, lines 27-29.) The dependent claims recite additional features, such as in claim 2 where it is stated that "the voltage signal on the one-wire bus includes a bias signal equal to the reference voltage level." (See page 6, lines 13-15.)

The Pryor patent does not show each and every element and limitation of the claims as amended. In the Office Action, the Examiner characterized Pryor as showing an active pull-up device (P12) and a level shift circuit (N12) connected to a one-wire bus (wire 46 connected to P12, N12). An excerpt of FIG. 1 in Pryor showing these components is provided below. Operation of this circuit is explained in Pryor at Col. 3, line 67 – Col. 4, line 19: "When Vc is low, N11 is turned-off and P11 is turned on. The turn-on of P11 turns-off P12. [Note that the patent incorrectly states "P1"and "P2" – it should be "P11" and "P12," respectively.] There is no current into N12 and no bias voltage is developed." With respect to FIG. 1 below, in this state current Ib = 0, and since there is no current into N12 (N12 is turned off), Vb = 0V. Further,

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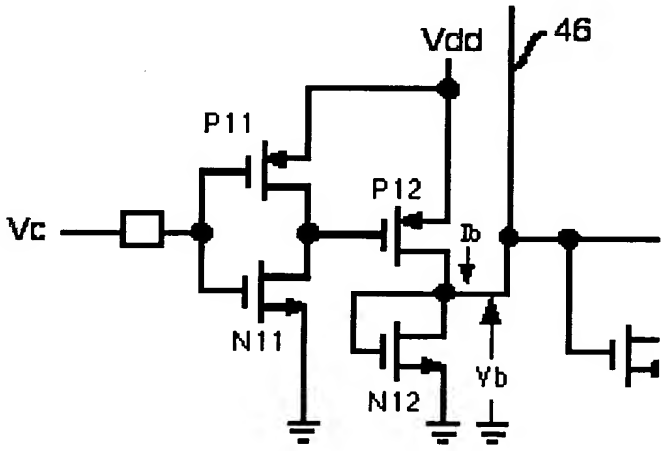
[1] Note that this is characterized in claim 1 as "the active pull-up device is configured to decrease the transition time of a voltage signal on the one-wire bus transitioning from a first voltage level to a second, higher voltage level," and in claim 7 as "the active pull-up device is configured to output a first designated voltage level on the one-wire bus when a measured voltage level of a communication signal on the bus rises above a second designated voltage level."

[2] Again, in claim 1 this is characterized as "the active pull-up device is configured to operate with respect to the constant reference voltage level for decreasing the transition time of said voltage signal," and in claim 7 as "said active pull-up device measuring the voltage level of the communication signal with respect to the constant reference voltage level."

"when Vc is 'high' P11 is turned-off and N11 is turned-on clamping the gate of P12 at, or close to, ground potential and causing a current Ib to flow through P12 and into the drain-to-source path of N12. A voltage Vb is then generated across the drain/gate and source of N12..." With a current Ib > 0, N12 is turned on, establishing a voltage Vb > 0 V.



Excerpt of FIG. 1 from Pryor

As should be appreciated, this circuit does not function in a manner as recited in the present claims. The state of transistor P12 (on or off) determines whether there is a current Ib, whether N12 is on or off, and whether Vb = 0V or Vb > 0V. Transistor P12 is not configured to cause a faster transition of a low-to-high voltage signal on line 46 (claim 1), and does not measure the voltage level on line 46 (claims 3 and 7). Moreover, transistor P12 does not operate with respect to a voltage established by transistor N12. Instead, the state of transistor P12, as determined from the inverter pair P11, N11, determines whether Vb is at ground or a positive voltage. Finally, transistor N12 does not establish a constant reference voltage. As explained, depending on the state of transistor P12, the voltage established across N12 varies from 0V (when N12 is off) to some positive voltage (when N12 is on).

In light of the above, the Applicants submit that Pryor does not show every element and limitation of claims 1 and 7. As such, claims 1 and 7 are

believed allowable over Pryor. Claims 2-6, 8, and 11-13, which depend from claims 1 and 7, are believed allowable as depending from allowable base claims. The dependent claims are further believed allowable as reciting additional elements not shown in Pryor. For example, in Pryor the voltage signal on line 46 is not biased by a constant reference voltage, and any devices connected to the line 46 are not configured to operate with respect to the constant reference bias voltage different than ground/0V (claims 2, 5, 6, 8, 11, and 13). Instead, line 46 is either at 0V when N12 is off or at Vb > 0V when N12 is on. There is no bias voltage of the signal on line 46.

Claims 1-13 were also rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Pat. No. 6,535,026 to Chung et al. ("Chung"). In light of the amendments above, it is believed that Chung does not anticipate the invention as recited in the pending claims.

In the Office Action, the Examiner characterized transistor 96 in FIG. 3B in Chung as an active pull-up device, transistor 102 as a level shift circuit, and the wire connected to SA and Vz as a one-wire bus. FIG. 3B is replicated below:

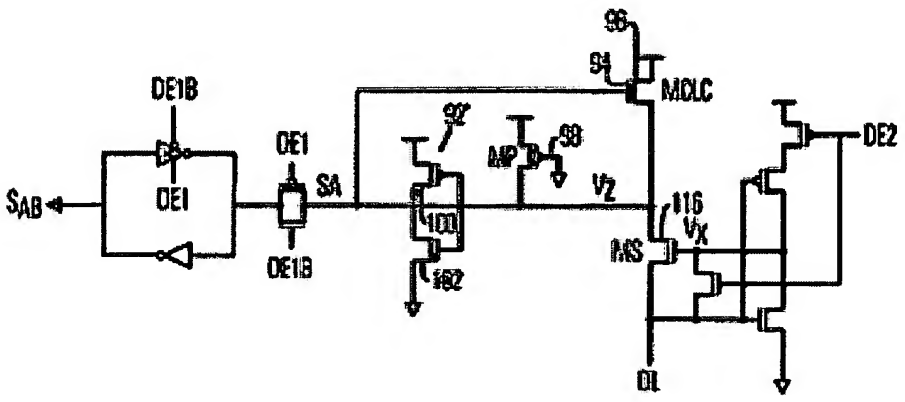


FIG. 3B

First, it should be noted that there is no line connecting points SA and Vz. Reference is made to the certificate of correction in Chung, which states that the cross-line between transistors 100 and 102 is an error:

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,535,026 B2 Page 1 of 1
DATED : March 18, 2003
INVENTOR(S) : Cheng-Lin Chuag and Nien-Chao Yang

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page and Drawings
Sheet 5 of 8, Figure 3B, please delete the horizontal line directly above reference numeral 100.

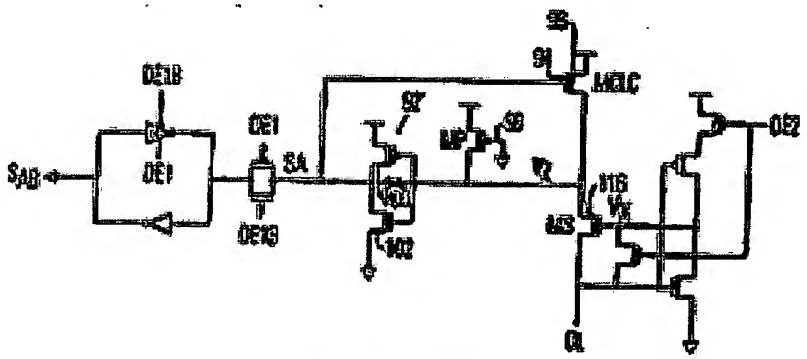


FIG. 3B

As such, this does not constitute a one-wire bus. Moreover, this circuit operates in the following manner: "The inverter 92 also inverts the data output Vz to SA. When the transfer bias voltage Vx turns on the pass transistor 116, a dropping data output Vz level will raise SA, which will turn on the precharge transistor 96 more and cause the data output Vz level to increase. Conversely, if the data output Vz level raises, then SA drops, turning off the precharge transistor 96 and allowing Vz to fall." Col. 8, line 58 – Col. 9, line 22. Transistor 96 is not configured to cause a faster transition of a low-to-high voltage signal on either line Vz or SA (claim 1), and does not measure the voltage level on either line Vz or SA (claims 3 and 7). Instead, when voltage level Vz falls, transistor 96 causes Vz to rise, and when Vz rises, transistor 96 causes Vz to fall. Still further, transistor 96 does not operate with respect to a voltage established by transistor 102 (the purported level shift

circuit), and transistor 102 does not establish a constant reference voltage. Note that transistor 102 is part of an inverter 92, 92'. When Vz is high, transistor 102 is on and the voltage level on SA is low/0V. When Vz is low, transistor 102 is off and the voltage level on SA is high. The voltage across transistor 102 varies, and does not establish a constant reference voltage. Finally, there is no bias voltage of communication signals on either line Vz or SA.

In light of the above, it is submitted that Chung does not disclose all the elements recited in Claims 1-8 and 11-13 as amended. Accordingly, these claims are believed allowable under 35 U.S.C. § 102(b).

NEW CLAIM 14

Independent claim 14 is newly added, and is believed allowable over Chung and Pryor for reasons similar to those set forth above. In particular, claim 14 includes elements similar to the other independent claims 1 and 7.

CONCLUSION

In view of the foregoing, it is respectfully submitted that pending claims 1-8 and 11-14 are in condition for allowance and action to that effect is earnestly solicited.

Pursuant to 37 C.F.R. § 1.136, the Applicants hereby petition for a one-month of extension of time, thereby extending the period for response to and through March 20, 2006. Authorization is hereby given to charge any fees owed to our Deposit account No. 13-0235.

Respectfully submitted,

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